

<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  (Use several sheets if necessary)	Attorney Docket No.: <b>4001-1201</b>	Application No.: <b>10/532,643</b>
	Applicant: <b>Christian SIEMERS</b>	
	Filing Date: <b>April 25, 2005</b>	Group Art Unit: <b>2819</b>

**U.S. PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing date (if appropriate)
JC	2002/0143505					
JC	2002/443505	10/3/2002	DRUSINSKY			
JC	4,870,302	9/26/1989	FREEMAN			

**FOREIGN PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation
						Yes No
JC	WO 00/69072	11/16/2000	INTERNATIONAL			

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

JC	SIEMERS C ET AL.; "Reconfigurable computing based on universal configurable blocks-a new approach for supporting performance- and realtime-dominated applications", COMPUTER ARCHITECTURE CONFERENCE, 2000. ACAC 2000. 5 <sup>TH</sup> AUSTRALASIAN CANBERRA, ACT, AUSTRALIA 31 JAN. - 3 FEB. 2000, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 31 January 2000 (2000-01-31), pages 82-89, XP010370824 ISBN: 0-7695-0512-0, Paragraphen 4.3 und 4.4, figures 4,5					
JC	SKLYAROV V.; "Reconfigurable models of finite state machines and their implementation in FPGAs", JOURNAL OF SYSTEMS ARCHITECTURE, ELSVIER SCIENCE PUBLISHERS BV., AMSTERDAM, NL, vol. 47, no. 14-15, August 2002 92002-08), pages 1043-1064, XP004375020, ISSN: 1383-7621, paragraphen 6 mit 10 figures 8c, 10					
JC	CHIEN A A ET AL.; "MORPH: a system architecture for robust high performance using customization (an NSF 100 TeraOps point design study)", FRONTIERS OF MASSIVELY PARALLEL COMPUTING, 1996. PROCEEDINGS FRONTIERS '96., SIXTH SYMPOSIUM ON THE ANNAPOLIS, MA, USA 27-31 OCT. 1996, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 27 October 1996 (1996-10-27), pages 336-345, XP010201607, ISBN: 0-8186-7551-9, the whole document					
JC	RABAEY J M; "Hybrid reconfigurable processors-the road to low-power consumption", VLSI DESIGN, 1998. PROCEEDINGS., 1998 ELEVENTH INTERNATIONAL CONFERENCE ON CHENNAI, INDIA 4-7 JAN. 1998, LOS ALAMITOS, CA USA, IEEE COMPUT. SOC, US, 4 January 1998 (1998-01-04), pages 300-303, XP010263449, ISBN: 0-8186-8224-8, Abschnitt "4. THE BERKELEY PLEIADES PROJECT", figure 5					
JC	DEVADAS S ET AL.; "DECOMPOSITION AND FACTORIZATION OF SEQUENTIAL FINITE STATE MACHINES", IEEE TRANSACTIONS ON COMPUTER AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE INC. NEW YORK, US, vol. 8, no. 11, 1 November 1989 (1989-11-01), pages 1206-1217, XP000126892, ISSN: 0278-0070, the whole document					
JC	P.M. HEYSTERS, J.M. SMIT, B. MOLENKAMP; "Reconfigurable Architecture for Handheld Devices", PROCEEDINGS OF THE 3D PROGRESS WORKSHOP ON EMBEDDED SYSTEMS, 24 October 2002 (2002-10-24), XP002295073 UTRECHT, the whole document					
JC	C. SIEMERS; "Configurable Computing - Ansätze, Chancen und Herausforderungen", TAGUNGSBAND EMBEDDED WORLD 2003, February 2003 (2003-02), pages 631-648, XP002295074, Abschnitt "4. Entwicklungsmethodik für Reconfigurable Computing", figures 16					
JC	M KOSTER, J. TEICH; "(Self-)reconfigurable Finite State Machines: Theory and Implementation", PROCEEDINGS OF THE 2002 DESIGN AUTOMATION AND TEST IN EUROPE CONFERENCE AND EXHIBITION, 4 March 2002 (2002-03-04), pages 1-8, XP002295075 PARIS, the whole document					
JC	TESSIER R ET AL.; "RECONFIGURABLE COMPUTING FOR DIGITAL SIGNAL PROCESSING: A SURVEY", JOURNAL OF VLSI SIGNAL PROCESSING SYSTEMS FOR SIGNAL, IMAGE, AND VIDEO TECHNOLOGY, KLUWER ACADEMIC PUBLISHERS, DORDRECHT, NL, vol. 28 no. 1/2, May 2001 (2001-05), pages 7-27, XP001116960, ISSN: 0922-5773, pages 21-22; figures 6, 7					

JC	C.SIEMERS, S. WENIGERS: "The Universal Configurable Block/MACHINE System - An Approach for a Homogeneous Configurable Soc-Architecture", PROCEEDINGS OF THE WORKSHOP HETEROGENEOUS RECONFIGURABLE SYSTEMS ON CHIP - SOC, February 2002 (2002-02), pages 1-6, XP002295076, HAMBURG figure 4
JC	E. CANTO ET AL.: "A Temporal Bipartitioning Algorithm for Dynamically Reconfigurable FPGAs", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION - VLSI - SYSTEMS, vol. 9, no. 1, February 2001 (2001-02), pages 210-218, XP002295077, the whole document
JC	HARTENSTEIN R: "Coarse grain reconfigurable architectures", CONFERENCE PROCEEDINGS ARTICLE, 30 January 2001 (2001-01-30), pages 564-569, XP010537867, the whole document
EXAMINER: /Jason Crawford/	
DATE CONSIDERED 08/07/2006	
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.	

\* English language abstract provided for the Examiner's convenience

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